A fully integrated 4.8-6 GHz Power Amplifier with on-chip output balun in 38 GHz-f_T Si-Bipolar

Student paper

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Abstract **A fully integrated radio frequency power amplifier for 4.8-6 GHz has been realized in a 38 GHz-f_T, 0.25 μm- Si-BiCMOS technology. The balanced 2-stage push-pull power amplifier uses two on-chip transformers as input balun and for interstage matching and an LC-type output balun with planar inductors. With this output network no external elements are required. At 1.2 V, 1.5 V, 2 V supply voltages output powers of 17 dBm, 18.9 dBm, 20.7 dBm are achieved at 5.8 GHz. The small-signal gain is 23 dB.**

I. Introduction

With the boom of wireless LAN chipsets the need of power amplifer solutions for low supply voltage arises. In the past serveral such power amplifiers for low power voltages have been reported [1], [2], but most of them require an external matching circuitry or do not fit the 5 GHz band. Beside the often found single-ended power amplifiers [3], the only reported differential typed amplifier with an integrated single-ended output solution was presented in [4] for 2.4 GHz in CMOS.

Aim of the work presented here was to realize a fully integrated power amplifier for the 4.8-6 GHz band with no external elements needed. The amplifier circuit is based on two on-chip transformers for the input balun and for interstage matching. The push-pull type circuit configuration, invented in the early days of tubes, has survived into semiconductor era with its benefits. The concept shows a 4:1 load-line impedance benefit for a push-pull combining scheme in an equal power comparison to a single-ended design. This is an advantageous issue at low supply voltages. However, usually an output balun is required. Impedance mismatch losses at the output of an RF power amplifier due to the decrease of the impedance required at low power supply voltages, conduction losses, charge-storage effects of the transistor and the contrary behaviour of gain and switching speed vs. breakdown voltage limits the maximum available output power and PAE. Therefore, for the first time, an LC-type balun was integrated on-chip including RF-choke and DC-block capacitor to achieve a single-ended 50 Ω output.

II. Circuit Design

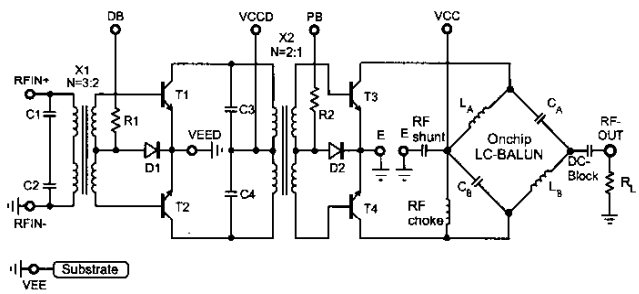

Fig. 1. Circuit diagram of the fully integrated power amplifier.

Fig. 1 shows the circuit diagram of the power amplifier. The circuit consists of a transformer X1 as input balun, a driver stage T1 and T2, a transformer X2 as interstage matching network and the output stage T3 and T4. The bias of the driver stage and the output stage are set by current mirrors D1 and D2, respectively. The effective emitter area of T1, T2 is 40 μm^2 and 100 μm^2 for T3, T4 each.

X1 is connected as a parallel resonant device with the input capacitors C1 and C2. The transformer acts as balun as well as input matching network. In addition there are several advantages:

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- No restrictions to the external DC potential at the input terminals.
- No external DC-block capacitor required.
- The input signal can be applied balanced or unbalanced if one input terminal is grounded.
- Relaxed electrostatic discharge requirements.

The turn ratio of X1 is N=3:2. The size is 165 x 165 μm^2. The primary winding consists of 3 turns. Metal 1 and Metal 2 are not used to reduce parasitic substrate coupling of the primary winding. Both turns of the secondary winding use also metal 3. The total coupling coefficient is k = 0.7 at 5.8 GHz.

Fig. 2 shows the interstage power transformer. X2 is connected as a parallel resonant device with two capacitors C3 and C4. C3 and C4 are connected in antiseries to short the parasitic substrate capacities to the VCCD node. X2 has a turn ratio of N=2:1. The total coupling coefficient is k = 0.45 at 5.8 GHz. The size is 150 x 150 μm^2. The primary winding consists of 2 turns with metal 3 and the secondary of 1 turn also using metal 3 . Modeling issues of monolithic transformers are presented in [5], [6], [7], [8].

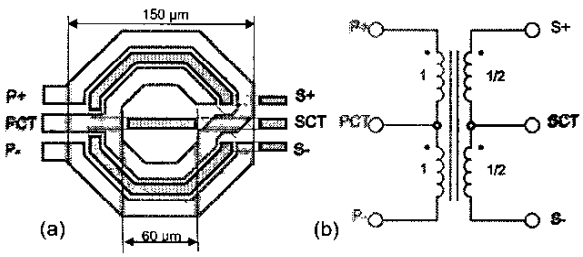

Fig. 2. Interstage power transformer X2: (a) Winding scheme (b) Schematic symbol.

III. On-chip LC-Balun design

During last years several balun concepts have been proposed [9], [10], but most of them result in large structures. The Lattice-type LC-balun [11], [12] is the most compact solution, as it is a solution based on lumped components. Additionally it allows also an impedance transformation and can be realized using transmission lines [13].

The ideal lattice-type balun consists of two inductances $L_A = L_B$ and two capacitors $C_A = C_B$ (Fig. 1). An RF-choke and a DC-block capacitor are used to feed the supply voltage to the collectors. R_1 is the balanced input impedance of the bridge. Each collector is loaded by $R_1/2$. R_L is the load resistor, usually 50 Ω. L and C can be calculated by

$$L_A = L_B = \frac{Z_1}{\omega_1} \quad (1)$$

$$C_A = C_B = \frac{1}{\omega_1 Z_1} \quad (2)$$

where $Z_1 = \sqrt{R_1 \cdot R_L}$ is the characteristic impedance of the bridge. $\omega_1 = 2\pi f_1$ is the frequency of operation.

Unfortunately, the use of bond wires at the RF output leads to a complex valued load impedance. So we use the series circuit of bond-wire and the DC-block capacitor to get a real-valued load. With the knowledge of this real-valued load, the LC-balun can be designed using equations 1 and 2. Interconnections, inductances and parasitic capacitances will shift the calculated values for L and C. Additionally, bond wires for the power supply feeding have to be considered as well as the transmission lines at the balun input.

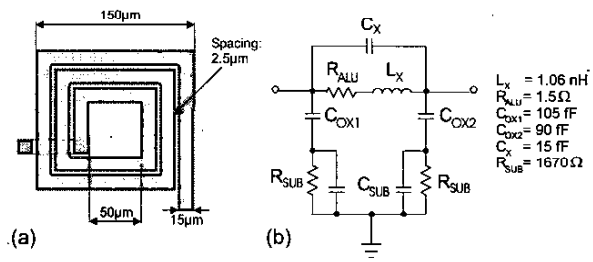

Fig. 3. (a) 1nH Coil (b) Equivalent circuit.

Fig. 3 shows the used coils L_A and L_B.The size is 150 x 135 μm^2. The winding consists of 2.75 turns. metal 1 and metal 2 are not used to reduce parasitic substrate coupling of the winding. The interconnection uses Metal 1 and 2 to have about the same maximum current density applicable. The inductors are modeled with an in-house tool called Coilgen based on Grovers formula [14] and substrate effects presented in [7], [15]. The equivalent circuit for the used coils L_A and L_B can be found in Fig. 4. Capacitances and DC-block were realized as *metal/isolator/metal* capacitors (MIM-CAPs).

IV. Technology

Fig. 4 shows the die photograph of the fully integrated power amplifier. The die size is 0.9 x 1 mm^2.

The technology used in this work is a 0.25 μm BiCMOS process. It features a bipolar junction transistor with an f_T of 38 GHz and a three layer metalization with an optional thick upper layer, used for this chip. Further devices

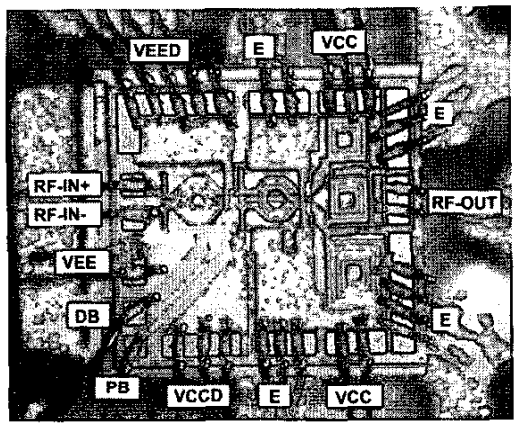

Fig. 4. Die Photograph of the power amplifier (size: $0.9 \times 1\,\mathrm{mm}^2$).

are a vertical pnp transistor, poly-Si resistors, MIM capacitors and inductors. The worst-case collector-base breakdown voltage is BVCB0 = 8 V (typical 12 V) and the worst-case collector-emitter breakdown voltage is BVCE0 = 2.6 V (typical 3 V).

V. Experimental Results

Fig. 5 shows the power amplifier test-board. The substrate parameters are $\varepsilon_r = 3.38$, $\tan\delta = 0.0027$ and the dielectric thickness is 0.51 mm. The metalization layers consist of 18 μm copper with a nickel diffusion barrier and 5 μm gold on top for bonding. The die is attached with a conductive epoxy to the substrate and is bonded directly on the board.

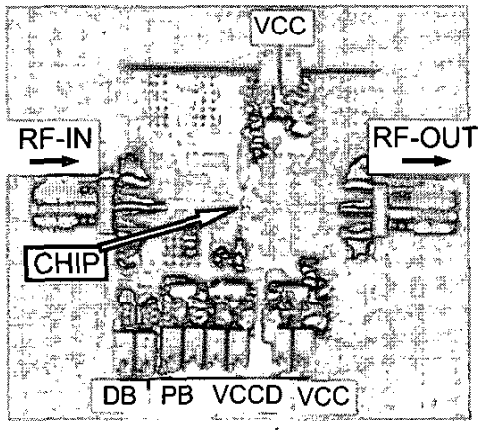

Fig. 5. Photograph of the power amplifier test board (size: $30 \times 30\,\mathrm{mm}^2$).

The power amplifier was characterized operating in a pulsed mode with a duty cycle of 12.5% with a pulse width of 600 μs as well as for CW operation (Tab. I).

Fig. 6 shows the measured power transfer characteristic. The maximum output power is 20.7 dBm at 2.0 V supply voltage and 5.8 GHz. The maximum PAE is 14.2%. Fig. 7 shows the characteristic vs. the supply voltage. The linearity for wireless LAN applications was tested using an WLAN-OFDM Error Vector Magnitude measurement setup in CW-mode: The EVM of 3 % is reached for an input power of -8 dBm, next to the compression.

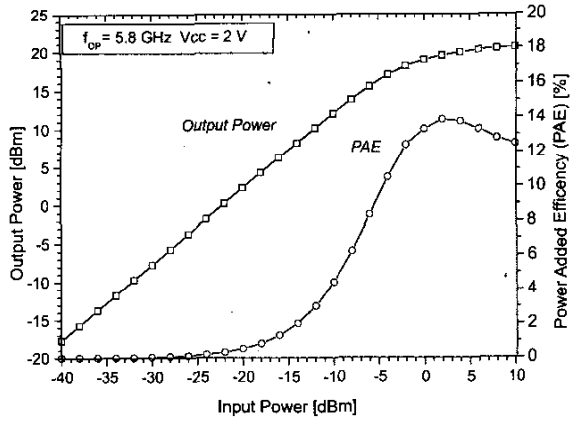

Fig. 6. Measured power transfer characteristic (T=300 K, 12.5 % duty cycle, 0.600 ms pulse width).

Fig. 8 shows the frequency response. The frequency response shows a high PAE and output power level in a frequency range from f = 4.8 GHz to 6 GHz. Tab. I shows the performance summary.

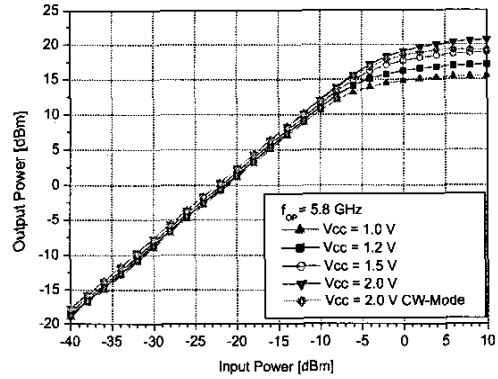

Fig. 7. Measured power transfer characteristic vs. supply voltage.

Operating frequency	4.8 GHz – 6 GHz					
Small-signal gain	23 dB					
Supply voltage	1	1.2	1.5	2.0	2.0 CW	V
Maximum output power (5.8 GHz, Pin=10 dBm)	15.5 (36)	17 (50.2)	18.9 (77.6)	20.7 (118)	19.3 (85.2)	dBm mW
Power-added efficiency (5.8 GHz, Pin=0 dBm)	13	14	14.2	14	11	%
Output stage collector current (RF on) + bias	150 + 16	170 + 16	197 + 16	230 + 16	250 + 13.7	mA
Output stage collector current (RF off) + bias	76 + 16	79 + 16	85 + 16	96 + 16	78 + 14.6	mA
Driver stage current (RF on) + bias	50 + 8	52 + 8	55 + 8	55 + 8	78 + 13.6	mA
Driver stage current (RF off) + bias	33 + 8	35 + 8	37 + 8	42 + 8	100 + 12.5	mA

TABLE I. Performance Summary (T=300 K, 12.5 % duty cycle, 0.600 ms pulse width - CW: continious wave.)

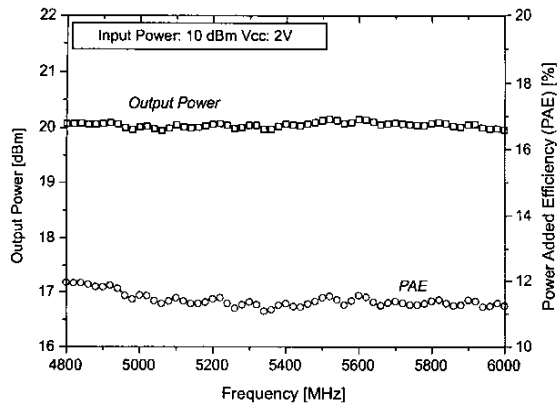

Fig. 8. Measured power amplifier frequency characteristic.

VI. Conclusions

We have demonstrated a low voltage power amplifier for 4.8-6 GHz in a 0.25 μm-Si-bipolar technology. It is based on a push-pull type circuit with on-chip transformer coupling and on-chip output balun. Thus the amplifier doesn't require any external elements and shows a wide bandwidth of over 1 GHz with a deviation of < 0.3 dB. In CW mode and a supply voltage of 2 V the output power is 19.3 dBm at 5.8 GHz. The maximum output power is 20.7 dBm at 2 V supply voltage. The small signal gain is 23 dB.

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